Remarks

Claims 6-9 and 25 are now pending in this application. Claims 6-9 are rejected. Claim 5 is objected to. Claims 1-5 and 10-24 are canceled without prejudice, waiver, or disclaimer. Claims 6 and 8 have been amended. Claim 25 is newly added. No new matter has been added. No fees are due for the newly added claim.

The objection to Claim 5 is respectfully traversed. Applicant has canceled Claim 5. Accordingly, Applicant respectfully requests that the objection to Claim 5 be withdrawn.

The rejection of Claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Biard (U.S. Patent No. 4,661,726) is respectfully traversed.

Biard describes a buffered FET logic (BFL) gate utilizing a temperature compensation scheme. The BFL gate includes a plurality of MESFETs (30-37) (Figure 4). In this circuit, temperature compensation is provided by the MESFETs (33, 34, 35, and 36) working in conjunction with the MESFET (37). Those skilled in the art will readily perceive that the invention may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's). At crossover, the gate to source voltage of the transistor (32) is reverse biased and is equal to -0.93 V. An output crossover voltage for the circuit is -0.293 V at 25° C with a temperature dependence of 0.37 mV/°C.

Applicant respectfully submits that the Section 103 rejection of Claim 6 is not a proper rejection. As is well established, the mere assertion that it would have been obvious to one of ordinary skill in the art to have modified Biard to obtain the claimed recitations of the present invention does not support a prima facie obvious rejection. Rather, each allegation of what would have been an obvious matter of design choice must always be supported by citation to some reference work recognized as standard in the pertinent art and the Applicant given the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference. Applicant has not been provided with the citation to any reference supporting the combination made in the rejection. The rejection, therefore, fails to provide the Applicant with a

fair opportunity to respond to the rejection, and fails to provide the Applicant with the opportunity to challenge the correctness of the rejection. Of course, such combinations are impermissible, and for this reason alone, Applicant requests that the Section 103 rejection of Claims 6 be withdrawn.

Further, and to the extent understood, Biard does not describe or suggest the claimed combination, and as such, the presently pending claims are patentably distinguishable from the cited combination. Specifically, Claim 6 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an input; an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output; a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel; a first output at an electrical node between said voltage drop circuit and said first channel, wherein said first output is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output; and a second output at an electrical node between said voltage drop circuit and said second channel."

Biard does not describe or suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit recited in Claim 6. Specifically, Biard does not describe or suggest the BFL level-shifting/inverting circuit including a first output at an electrical node between the voltage drop circuit and the first channel, where the first output is coupled to a chopping circuit configured to chop a signal based on a signal received at the first output. Rather, Biard describe a buffered FET logic (BFL) gate including a plurality of MESFETs. The BFL logic gate may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors. An output crossover voltage for the BFL gate is -0.293 V at 25° C with a temperature dependence of 0.37 mV/°C. Accordingly, Biard does not describe or suggest the first output that is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output. For the reasons set forth above, Claim 6 is submitted to be patentable over Biard.

For at least the reasons set forth above, Applicant respectfully requests that the Section 103 rejection of Claim 6 be withdrawn.

The rejection of Claim 7 under 35 U.S.C. § 103(a) as being unpatentable over Biard and further in view of Tohyama (U.S. Patent No. 4,810,907) is respectfully traversed.

Biard is described above. Tohyama describes a circuit including MESFETs Q_1 and Q_2, with a resistor R therebetween. The MESFETs and the resistor are connected in series between a drain supply voltage V_{DD} and a ground. The transistor Q_2 is a normally an ON type FET. The circuit has an output terminal (2).

Claim 7 depends on independent Claim 6 which recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an input; an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output; a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel; a first output at an electrical node between said voltage drop circuit and said first channel, wherein said first output is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output; and a second output at an electrical node between said voltage drop circuit and said second channel."

Neither Biard nor Tohyama, considered alone or in combination, describe or suggest a buffered field effect transistor logic (BFL) level-shifting/inverter circuit recited in Claim 6. Specifically, neither Biard nor Tohyama, considered alone or in combination, describe or suggest the BFL level-shifting/inverting circuit including a first output at an electrical node between the voltage drop circuit and the first channel, where the first output is coupled to a chopping circuit configured to chop a signal based on a signal received at the first output. Rather, Biard describe a buffered FET logic (BFL) gate including a plurality of MESFETs. The BFL logic gate may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide

semiconductor field effect transistors. An output crossover voltage for the BFL gate is -0.293 V at 25° C with a temperature dependence of 0.37 mV/°C. Tohyama describes a circuit including MESFETs Q_1 and Q_2, with a resistor R therebetween. The circuit has an output terminal. Accordingly, neither Biard nor Tohyama, considered alone or in combination, describe or suggest the first output that is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output. For the reasons set forth above, Claim 6 is submitted to be patentable over Biard and further in view of Tohyama.

When the recitations of Claim 7 are considered in combination with the recitations of Claim 6, Applicant submits that dependent Claim 7 likewise is patentable over Biard and further in view of Tohyama.

For at least the reasons set forth above, Applicant respectfully requests that the Section 103 rejection of Claim 7 be withdrawn.

The rejection of Claims 8 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Biard and further in view of Tohyama and Alok et al. (U.S. Patent No. 6,559,068), referred to as Alok, is respectfully traversed.

Biard and Tohyama are described above. Alok describes a system and a method for improving inversion layer mobility in a silicon carbide metal-oxide semiconductor field-effect transistor (MOSFET). The method includes positioning a silicon carbide substrate and metallic impurities in a chamber, and forming an oxide layer on a surface of the silicon carbide substrate by introducing nitrogen gas bubbled through deionized water into the chamber.

Claim 8 recites a buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising "an inverter stage input; an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output; a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel; and a resistor electrically connected in series between said first channel and said second channel; a first output

at an electrical node between said resistor and said first channel, wherein said first output is coupled to a chopping circuit configured to chop a signal based on a signal received at said first output; and a second output at an electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate."

None of Biard, Tohyama, and Alok, considered alone or in combination, describes or suggests a buffered field effect transistor logic (BFL) level-shifting/inverter circuit recited in Claim 8. Specifically, none of Biard, Tohyama, and Alok, considered alone or in combination, describes or suggests the BFL level-shifting/inverting circuit including a first output at an electrical node between the resistor and the first channel, where the first output is coupled to a chopping circuit configured to chop a signal based on a signal received at the first output. Rather, Biard describe a buffered FET logic (BFL) gate including a plurality of MESFETs. The BFL logic gate may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors. An output crossover voltage for the BFL gate is -0.293 V at 25° C with a temperature dependence of 0.37 mV/°C. Tohyama describes a circuit including MESFETs Q_1 and Q_2, with a resistor R therebetween. The circuit has an output terminal. Alok describes a silicon carbide substrate and metallic impurities, which are positioned in a chamber. An oxide layer is formed on a surface of the silicon carbide substrate by introducing nitrogen gas bubbled through deionized water into the chamber. Accordingly, none of Biard, Tohyama, and Alok, considered alone or in combination, describes or suggests the first output that is coupled to a chopping circuit configured to chop a signal based on a signal received at the first output. For the reasons set forth above, Claim 8 is submitted to be patentable over Biard and further in view of Tohyama and Alok.

Claim 9 depends on independent Claim 8. When the recitations of Claim 9 are considered in combination with the recitations of Claim 8, Applicant submits that dependent Claim 9 likewise is patentable over Biard and further in view of Tohyama and Alok.

For at least the reasons set forth above, Applicant respectfully requests that the Section 103 rejection of Claims 8 and 9 be withdrawn.

Moreover, Applicant respectfully submits that the Section 103 rejections of Claims 7-9 are not proper rejections. As is well established, obviousness cannot be established by combining the teachings of the cited art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Biard, Tohyama, and Alok, considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicant respectfully submits that it would not be obvious to one skilled in the art to combine Biard with Tohyama or Alok because there is no motivation to combine the references suggested in the cited art itself.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicant's disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion nor motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejections are based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, Biard teaches a buffered FET logic (BFL) gate including a plurality of MESFETs. The BFL logic gate may be used with any logic

gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors. An output crossover voltage for the BFL gate is -0.293 V at 25° C with a temperature dependence of 0.37 mV/°C. Tohyama teaches a circuit including MESFETs Q_1 and Q_2, with a resistor R therebetween. The circuit has an output terminal. Alok teaches a silicon carbide substrate and metallic impurities, which are positioned in a chamber. An oxide layer is formed on a surface of the silicon carbide substrate by introducing nitrogen gas bubbled through deionized water into the chamber. Since there is no teaching nor suggestion in the cited art for the combination, the Section 103 rejections appear to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicant requests that the Section 103 rejections of Claims 7-9 be withdrawn.

For at least the reasons set forth above, Applicant respectfully requests that the rejections of Claims 7-9 under 35 U.S.C. 103(a) be withdrawn.

Newly added Claim 25 depends from independent Claim 6, which is submitted to be in condition for allowance and is patentable over the cited art. For at least the reasons set forth above, Applicant respectfully submits that Claim 25 is also patentable over the cited art.

In view of the foregoing amendment and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,

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